WHAT IS CLAIMED IS:

1. An in-situ deposition and doping method for a polycrystalline silicon layer of a semiconductor device, said method comprising the steps of:

growing a first intermediate layer of in-situ doped polycrystalline silicon with a first doping level; and

growing a second additional layer of polycrystalline silicon with a second doping level that is lower than the first doping level.

2. The in-situ deposition and doping method as defined in claim 1, wherein the second doping level is substantially lower than the first doping level.

3. The in-situ deposition and doping method as defined in claim 1, wherein the first intermediate layer and the second additional layer are of the same conductivity type.

4. The in-situ deposition and doping method as defined in claim 1, wherein both the first intermediate layer and the second additional layer have n-type conductivity.

5. The in-situ deposition and doping method as defined in claim 1, further comprising the step of purging dopant from the surrounding atmosphere, between the steps of growing a first intermediate layer and growing a second additional layer.

6. The in-situ deposition and doping method as defined in claim 1, wherein in the step of growing a first intermediate layer, a layer of polycrystalline silicon is produced with a thickness that is substantially at a 10:1 ratio with the thickness of the layer of polycrystalline silicon produced in the step of growing a second additional layer.

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7. The in-situ deposition and doping method as defined in claim 1, further comprising the step of performing a subsequent thermal treatment to diffuse dopant from the first intermediate layer to the second additional layer.

8. The in-situ deposition and doping method as defined in claim 1, wherein the step of growing a first intermediate layer is performed through an LPCVD process using a mixture of silane, hydrogen, and phosphine.

9. The in-situ deposition and doping method as defined in claim 8, wherein the step of growing a second additional layer is performed through an LPCVD process using a mixture of silane and hydrogen.

10. The in-situ deposition and doping method as defined in claim 1, wherein the second additional layer is substantially not doped.

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11. The in-situ deposition and doping method as defined in claim 10, further comprising the step of performing a subsequent thermal treatment to diffuse dopant from the first intermediate layer to the second additional layer.

12. The in-situ deposition and doping method as defined in claim 10, further comprising the step of performing a subsequent re-oxidation treatment to diffuse dopant from the first intermediate layer to the second additional layer.

13. The in-situ deposition and doping method as defined in claim 12, wherein the step of performing a subsequent re-oxidation treatment includes the sub-steps of:

performing a first thermal treatment in a non-oxidating environment to anneal generated defects; and

performing an oxidation treatment.

14. The in-situ deposition and doping method as defined in claim 10,

wherein the step of growing a first intermediate layer is performed through an LPCVD process using a mixture of silane, hydrogen, and phosphine, and

the step of growing a second additional layer is performed through an LPCVD process using a mixture of silane and hydrogen.

15. An in-situ deposition and doping method for a polycrystalline silicon layer of a semiconductor device, said method comprising the steps of:

growing a first intermediate layer of in-situ doped polycrystalline silicon with a first doping level;

growing a second additional layer of polycrystalline silicon with a second doping level that is lower than the first doping level; and

performing a re-oxidation thermal treatment to diffuse dopant from the first intermediate layer to the second additional layer,

wherein the second additional layer is substantially not doped.

16. The in-situ deposition and doping method as defined in claim 15, wherein the step of performing a re-oxidation thermal treatment includes the sub-steps of:

performing a first thermal treatment in a non-oxidating environment to anneal defects; and

performing an oxidation treatment.

17. A semiconductor memory device of the type having a gate stack, said memory device comprising:

at least one gate layer of polycrystalline silicon,

wherein the gate layer of polycrystalline silicon is formed from a first intermediate layer of polycrystalline silicon with a first doping level, and an overlaying second additional layer of polycrystalline silicon with a second doping level that is lower than the first doping level.

18. The memory device as defined in claim 17, wherein the second doping level is substantially lower than the first doping level.

19. The memory device as defined in claim 17, wherein the second additional layer is substantially not doped.

20. The memory device as defined in claim 17, wherein thermal treatment is used to diffuse dopant from the first intermediate layer to the second additional layer.

21. The memory device as defined in claim 17, wherein the memory device is a flash-type memory device.

22. A semiconductor memory device formed using an in-situ deposition and doping method for at least one polycrystalline silicon layer, said method comprising the steps of:

growing a first intermediate layer of in-situ doped polycrystalline silicon with a first doping level; and

growing a second additional layer of polycrystalline silicon with a second doping level that is lower than the first doping level.

23. The semiconductor memory device as defined in claim 22, wherein the second doping level is substantially lower than the first doping level.

24. The semiconductor memory device as defined in claim 22, wherein the second additional layer is substantially not doped.

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